# FEC Firmware Upgrade Tutorial

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# 1 FEC programming using the Xilinx Impact software

# 1.1 Installing the Xilinx Impact software

Go to the Xilinx.com website section Products -> Design Tools and download and install the free ISE WebPACK. If you have access to a full installation package (eg. CERN dfs) you can install the "Lab Tools" only, which will install Impact without the need to purchase or request a licence. The Xilinx software supports both Linux and Windows platforms.

You will also need to use the Xilinx Programmer cable (Platform Cable USB II)



You can find more information about alternative programming options from the Xilinx website, in the <u>Products – Technology - Configuration Solutions</u> section. In particular Digilent offers programming solutions compatible with the Xilinx software (for more details go to <u>http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,395&Cat=5</u>)

## 1.2 Connecting the Xilinx programming dongle to the FEC card

- a) Connect the Xilinx Programmer to the PC and wait until it is recognized and the corresponding drivers are automatically installed (Windows)
- b) Make sure the FEC card is switched off, then connect the flat cable of the Xilinx Programmer to the corresponding FEC connector (U15)



c) Power on the FEC card. If power conditions are ok, the light on the Xilinx Programmer will turn green.

## **1.3 Programming the FEC board**

a) Start the Impact software from the Start Menu:



b) Answer Yes when asked to create a project



c) Make sure that ... Boundary-Scan (JTAG) is selected and press OK

Welcome to iMPACT
Please select an action from the list below
Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable and identify Boundary-Scan chain
Prepare a PROM File
Prepare a System ACE File
Prepare a Boundary-Scan File
SVF 👻
OK Carrel

d) The program will automatically identify the devices EEPROM and FPGA devices present on the FEC JTAG chain. Press *No* when asked to automatically assign configuration files.

SE IMPACT (0.61xd) - [Boundary Scan]	23
File Edit View Operations Output Debug Window Help	- 8 ×
MPACT Flows ↔ □ ♂ × Right click device to select operations	
Boundary Scan     SystemACE     Create PROM File Format     WebTalk Data     Create PROM File Format     Create Provide Pro	
MPACT Processes ↔ G X	
Do you want to continue and assign configuration files(s)? Don't show this message again, save the setting in preference. Yes No	
Boundary Scan	
Console ++	□ & ×
<pre>(J.INFO:LMPACT:1777 - Reading C:/EDA/Xilinx/v13_2/ISE_DS/ISE/xcfp/data/xcf32p.bsd (J.INFO:LMPACT:501 - '1': Added Device xcf32p successfully</pre>	* III *
	P.
Configuration Parallel IV   5 MHz	LPT1

# e) Press OK to accept the default programming parameters

B Device Programming Properties - Device 1 P	rogramming Properties	X
Category		
Boundary-Scan Device 1 (PROM2 xcf32p)	Property Name	Value
Device 2 ( FPGA xc5vlx50t )	Verify	
	General CPLD And PROM Properties	
	Design-Specific Erase Before Programming	
	Read Protect	
	PROM/CoolRunner-II Usercode (8 Hex Digits)	
	PROM Specific Properties	
	Load FPGA	
· · · · · · · · · · · · · · · · · · ·	Parallel Mode	
	Advanced PROM Programming Properties	
	During Configuration: PROM is Configuration Master (check to select clock source)	
	[select clock source]	External Clock 👻
	During Configuration: PROM is Slave (clocked externally)	
	ОК	Cancel Apply Help

## 1.3.1 Temporarily programming the FEC FPGA

The firmware can be loaded directly into the FPGA without writing it permanently to the on-board EEPROM. This operation is useful for testing a new firmware update with minimum risk. At the next power cycle, the FPGA will boot with the default firmware stored on the local EEPROM. If you want to continue testing the new firmware you need to reload it to the FPGA.

If you want to permanently write the new firmware to the FEC board, go to next section (1.3.2 Program the on-borard boot EEPROM (permanent programming))

a) On the Boundary Scan tab right-click on the FPGA device (xc5vlx50t) and select Assign New Configuration File ...



b) In the new dialog, select the *.bit* file corresponding to the new firmware from the location where you unpacked the zip file downloaded from the web.

Computer	<ul> <li>System (C:)</li> <li>Documents</li> </ul>	Local + proms + fec_apz_v1_0b		<b>▼ 4</b> 9	Search fec_apz_v1_0b	
rganize 🔻 🛛 New folder	·				8== 👻	(
Favorites	Name	Date modified	Туре	Size		
📃 Desktop	fec_apz_top.bit	12/04/2012 16:29	BIT File	1,716 KB		
Downloads						
Public on DFS						
Recent Places						
smartoju						
Local						
-						
Libraries						
Documents						
🎝 Music 💷						
Pictures						
Subversion						
Videos						
Computer						
System (C:)						
DVD/CD-RW Driv						
📖 dfe (\\cern ch) (6 🍸						

c) Press No when asked to attach a SPI or BPI PROM



d) Right-click again on the FPGA device and select Program



/Documents/Local/proms/fec\_apz\_v1\_0b/fec\_apz\_top.bit' ...

e) Click OK to accept the default programming properties

Device Programming Properties - Device 2	Programming Properties	x
Category Boundary-Scan Device 1 (PROM2 xcf32p) Device 2 (FPGA xc5vb50t)	Property Name Value Verify	
	OK Cancel Apply Hel	p

f) Wait until Impact loads the firmware to the FPGA



- equency for this device chain: 15000000.
- g) If the programing procedure was successful Impact will display "Program Succeeded". You can now use the new firmware. Remember that the FPGA will revert to the old firmware after a power cycle or reboot command.

1						
Output	Debug	Window Help	)			
	<u>X</u> I	🖀 🔁 🗖 🖡	<i>▶</i> <b>k</b> ?			
ormat	TDI	xcf32p bypass	xc5vk50t fec_apz_top.bit			
- D & X	TDO					
					Program S	Succeeded
			Boundary S	Scan		
Brogram	mine	completed an	ccessfully			

### **1.3.2** Program the on-borard boot EEPROM (permanent programming)

a) On the Boundary Scan tab right-click on the EEPROM device (xcf32pt) and select Assign New Configuration File ...



b) In the new dialog, browse to the location where you unpacked the zip file downloaded from the web and select the *.mcs* file corresponding to the new firmware.

Assign New Configuration	File	local b prome b fac any vil Ob		- 4	aareh fas anz ul. Oh	
Computer	• system (c.) • bocuments •	cocar v proms v rec_apz_vi_ob		• • • • • • • • • • • • • • • • • • • •	earch rec_ap2_v1_ob	
Organize 🔻 New folder	r				•	
Pictures ^	Name	Date modified	Туре	Size		
Subversion	fec anz v1.mcs	13/04/2012 18:03	MCS File	5.633 KB		
🛃 Videos				5,055 110		
Connector						
System (C)						
DVD/CD-RW Driv						
🚽 dfs (\\cern.ch) (G						
🚽 cdslib (\\cern.ch						
📮 Network						
IBPC04						
IBPC05						
INPC06 ■						
PCALICEBHM12						
PCGS2X3160H60						
PCSCALA01						
PHOS100						
RD51HPC8000						
÷						
File na	me: fec_apz_v1.mcs			- All	Design Files (*.mcs '	*.isc *.bs 🤻
					Onen 🚽	Cancel

c) Right-click again on the EEPROM device and select Program



d) Wait until Impact loads the firmware to the EEPROM

Operations Output	Debug Window Help
\$\$ \$\$ 🛷 📑 🔳	<i>₽ №</i> ?
↔□₽×	
n	SPIJBPI
File (PROM File Format	
	xcf32p xc5vlx50t
	fec_apz_v1.mcs bypass TDO
******	
Ge Confi	guration Operation Status
Executin	ıg command
	20%
sum	Abort
ure/Usercode	
mer Code 👻	Boundary Scan

e) If the programing procedure was successful Impact will display "Program Succeeded". You can now power cycle the FEC board to load the new firmware from the boot EEPROM.

ISE iMPACT (0.61xd) - [Boundary Scan]		
File Edit View Operations Output	Debug Window Help	- 8 ×
		Lumphing Lump
MPACT Flows ++ D R X		
Boundary Scan     SystemACE     SystemACE     Crass Physics ACE     Crass Physics ACE     Web bik Data	TDI <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2000</b> <b>2</b>	
MPACT Processes ↔		
Available Operations are:		
Program		
Verify		
Blank Check		
Beadback	Program Succeeded	
Get Device ID	Togram Succeeded	
Get Device Checksum		
Get Device Signature/Usercode		
Get Device Customer Code 🗸 🗸	Boundary Scan	
Console		↔⊡∂×
'1': Putting device in ISP mod	dedone.	
done.		
done.		
'1': Putting device in ISP mod	iedone.	
done.		
'1': Programming completed suc	ccessfully.	
DECORPOSEEND For Completed Suc	scessiury.	
Flapsed time = 81 sec		
Liupsed time - bi sec.		
4		•
Errors 🔔 Warnings		
	Configuration Parallel IV 5 MHz	LPT1

# 1.4 Programming the FECv6 board

The JTAG connection of the FECv6 board is on the front-panel of the board, below the two DTCC RJ45 connectors.

... picture ...

To start the Impact programming tool you have to follow the same procedure as for the FECv3, as described in chapter 1.2. In this case, the main window of the tool will look like this:

Boundary Scan]	101	-		-	10.00	-	a Caller	
<u> </u>	Debug	<u>W</u> indow	<u>H</u> elp					_ & ×
🗋 🏓 🗐 🐰 🗎 ն 🗙 🏭 🎎	II 🔁	🔳 🖡 🄑	<b>k?</b>					
MPACT Flows ↔ □ 槽 ×								
Boundary Scan		(SP17	BPI					
Create PROM File (PROM File Format								
🔠 📄 WebTalk Data								
		xc6vi byp	x130t ass					
	TDO			J				
	1111							
MPACT Processes ↔ □	1000							
Available Operations are:	11111							
<ul> <li>Read eFUSE Registers</li> </ul>								
<ul> <li>Set eFUSE Control Register</li> <li>Read eFUSE Control Register</li> </ul>								
Get Device Signature/Usercode								
<ul> <li>Read Device Status</li> <li>Read Device DNA</li> </ul>					Identify S	Succee	ded	
	1		Bound	lary Scar	1			
Console								↔□₽×
PROGRESS_END - End Operation.								A
Elapsed time = 0 sec.	w							
// and BAICH CHD : Identifymp	14							-
<								- F
Console 😢 Errors 🔬 Warnings								
					Co	nfiguration	Platform Cable USB II	6 MHz usb-hs

## 1.4.1 Temporarily programming the FECv6 FPGA

The procedure is identical with the one described in chapter 1.3.1

#### **1.4.2** Program the on-borard boot EEPROM (permanent programming)

The FECv6 board uses a SPI flash chip which is not automatically detected by the tool.

a) Right click in the dotted rectangle on top of the FPGA icon where it is written "SPI/BPI ?", then click on the "Add SPI/BPI Flash..." menu item.

SE iMPACT (P.20131013) - [Boundary Scan]		
🐼 File Edit View Operations Output	Debug Window Help	_ 8 ×
🗋 ờ 🖶 🔓 🏭 📾 💥 🤀 🖻	<i>₽</i> k?	
MPACT Flows       ↔ □ ♂ ×         ↔ □ ♂ ×       ↔ □ ♂ ×         ↔ □ ♂ ×       ↔ □ ♂ ×         ↔ □ ♂ ×       ↔ □ ♂ ×         ↔ □ ♂ ×       ↔ □ ♂ ×         MPACT Processes       ↔ □ ♂ ×         Available Operations are:       ↔ □ ♂ ×	Right click device to select operations Add SPI/BPI Flash TDI	
	Boundary Scan	
Console		⇔⊡♂×
PROGRESS_END - End Operation. Elapsed time = 0 sec. // *** BATCH CMD : identifyMPP	м	
		•
Console 🛂 Errors 🚹 Warnings		
	Configuration Platform Ca	able USB II 6 MHz 1 usb-hs

## b) Select the .mcs file for the SPI programming

Add PROM File	a loss has been been			x
🔾 🗢 📕 « Documents	Local > FECv6_ADC > prom	← Search prom		٩
Organize 🔻 New folder				0
Documents	Name	Date modified	Туре	
Dropbox	fecv6_adc_v100.mcs	12/08/2014 17:43	MCS File	
Pictures				
Subversion				
Theos				
📢 Homegroup				
🖳 Computer				
🏭 OS (C:)				
DATA (D:)				
🖵 dfs (\\dfs.cern.ch				
☐ Microsoft Office	III			P.
File <u>n</u> an	ne: fecv6_adc_v100.mcs	✓ MCS Files (*.m.	cs)	•
		Open	Cance	

c) Leave "SPI PROM" as the type of PROM attached to the FPGA, and select the PROM part number from the drop-down list (the default prom used with the FECv6 board is S25FL128S; select another one if your board does not use the default one.)



d) Right click on the "FLASH" icon and select the "Program" menu item, then click "OK" in the Device Properties window. This will start the programming of the SPI flash. Do not power off or unplug the programming cable during this process.



#### 1.4.3 Creating the .mcs file necessary for permanent programming of the FECv6 board

If you do not have the .mcs files necessary to program the on-board SPI flash, or you have a different SPI flash, use the following procedure

a) Open the ISE Impact tool and double click on the "Create PROM File (PROM File Format..)" item in the Impact Flows list of the ISE Impact tool.



b) Select the "Configure Single FPGA" item under the "SPI Flash" category of Step 1, and then press on the green arrow on the right.

Step 1. Select Storage Tar	et Step 2.	Add Storage D	evice(s)		Step 3.		Enter Da	ata
Storage Device Type : - Xilinx Flash/PROM - Non-Volatile FPGA - SPI Flash - Configure Single FPGA - Configure Single FPGA - Configure MultiBoot FPGA - Configure MultiBoot FPGA - Configure from Paralleled PROMs - Generic Parallel PROM	Target FPGA Storage Device Add Storage	Spartan3E (bits): 512K - 2 Device Remove Store	v age Device	•	General File Detail Checksum Fill Value Output File Name Output File Location File Format Use Power-of-2 for Number of Bitstreau Bitstream 0 Start A Bitstream 1 Start A Add Non-Configura	FF Untitled C:\Xiinx\14.7\ e Property Start Addr m ddress ddress ddress e	Value ISE_DS\ Value BIN No 2 0 675840 Yes	
	Auto Select	t PROM			·····			•
Description:	1, select this storage device ty	/pe						

c) Select "128M" in the "Storage Device (bits)" list and then click on the "Add Storage Device" button followed by the green arrow button on the right.

tep 1.	Select Storage Target	Step 2.	Add Storage Device(s)	Step 3.	Enter Data
torage Device T	Type :	Storage Devis	ro (hita) 129M	General File Detail	Value
Xilinx Flash/P	ROM	Storage Devic	128K	Checksum Fill	
Spartan3	PGA BAN	Add Storag	256K torage Device	Output File Name Untitle	ed
Configur Configur	e Single FPGA e MultiBoot FPGA		1M 2M 4M	Output File Location	1x\14.7\ISE_DS\
Configur	e Single FPGA e MultiBoot FPGA		8M 16M 22M	Flash/PROM File Prope	erty Value
Configur	e from Paralleled PROMs		64M	File Format	BIN
Genericitara			128M	Use Power-of-2 for Start A	Addr No
			512M	Number of Bitstream	2
				Bitstream 0 Start Address	0
				Bitstream 1 Start Address	675840
				Add Non-Configuration Da	ta Files Yes
				Number of Data File	
		Auto Selec	ct PROM		
scription:					
• Storage • Add Store	will select the appropriate target device. e Device: This selection allows you to choose orage Device: After selecting the memory to e Storage Device: Use this button to delety device: After selecting the sel	e the specific device arget, use this butto e the target device	memory density you are targeting. In to add the device to the target Storage from the list below. Select the device and	Device list below. Lick this button to remove it from the	he list.

d) Change the "Output File Name" and "Output File Location" to the desired directory, then click OK.

Step 1. Select	t Storage Target	5	Step 2.	Add Storage Dev	vice(s)	-	Step 3.		Enter Dat
Storage Device Type : Xilmx Flash/PROM Non-Volatile FPGA Spt Flash Configure Single FPGA Configure MultBoot FPG BPI Flash Configure MultBoot FPG Configure MultBoot FPG Generic Parallel PROM	SA SA ed PROMs	•	Storage Device (bit Add Storage Dev 128M	n) 128M v ce Remove Storage		•	General File Detail Checksum Fill Value Output File Name Output File Location Flash/PROM Fil File Format Add Non-Configura	FF fecv6_adc_v1 :uments/Local/i e Property tion Data Files	Value
escription: in this step, you will enter infor	mation to assist in setting up an	nd ge	enerating a PROM file	for the targeted storage	device and m	ode.			
• Checksum Fill Value • Output File Name: Th	When data is insufficient to fill his allows you to specify the base	l the se na	entire memory of a F ame of the file to whi	ROM, the value specified th your PROM data will be	here is used t written	to calo	culate the checksun	n of the unused	portions.

## e) Click OK to start adding the device file:

B ISE iMPACT (P.20131013) - [PROM File Forma	atter: SPI Flash Single FPGA]	23
🛞 File Edit View Operations Output	Debug Window Help	- 8 ×
🗋 🍺 🛃 🛛 🔓 🐲 🖙 🖬 🥬 🧐		
iMPACT Flows ↔ □ & ×		*
Image: System ACE         Image: System ACE      <	C C C C C C C C C C C C C C	E
	Boundary Scan Brown File Formatter: SPI Flash Single FPGA	
Console		+□ ₽ ×
Number of PROMs : 1 PROM Name : 16M PROM S	Size : 16777216 bits ) of Report	•
Console Crrors Warnings		
PROM File Generation	larget SPI Flash   0 Bits used   File: fecv6_adc_v100 in Location: D:\Documents\Local\FECv6_ADC\prom/   u	sb-hs 🔡

f) Select and open the desired bit file

·		X
s ▶ Local ▶ FECv6_ADC ▶	✓ Search FECv6	5_ADC
		= - 1 0
Name	Date modified	Туре
🔐 .svn 🎉 _ngo	06/08/2014 19:47 05/08/2014 12:45	File folder File folder
_xmsgs iseconfig ising	06/08/2014 13:02 06/04/2014 08:01 06/08/2014 15:49	File folder File folder File folder
<ul> <li>isini</li> <li>prom</li> <li>remote_sources</li> </ul>	12/08/2014 17:33 02/04/2014 21:54	File folder File folder
sim Inx_auto_0_xdb st	06/08/2014 15:44 05/08/2014 12:41 05/08/2014 12:39	File folder File folder File folder
fecv6_adc_top.bit	05/08/2014 19:52	BIT File
(		•
ne: fecv6_adc_top.bit	✓ FPGA Bit Files Open	(*.bit)  Cancel
	s > Local > FECv6_ADC > Name svn go mgo msgs . iseconfig . isim . prom . remote_sources . sim . xlnx_auto_0_xdb xst . fecv6_adc_top.bit 	s > Local > FECv6_ADC > <ul> <li>4y</li> <li>Search FECv6</li> </ul> Name       Date modified         .svn       06/08/2014 19:47         _ngo       05/08/2014 19:47        ngo       05/08/2014 12:45        xmsgs       06/08/2014 13:02        iseconfig       06/04/2014 08:01

g) Click "No" to finalize the process of adding the design file

BE IMPACT (P.20131013) - [PROM File Forma	atter: SPI Flash Single FPGA]	23
🛞 File Edit View Operations Output	Debug Window Help	Ξ×
i 🗋 🎓 🛃 i 🔓 🏭 🚧 🖷 🖉 🔑 I	<i>k</i> ?	
IMPACT Flows     ↔ □ ∄ ×            ⊕ Boundary Scan             ⊕ SystemACE             ⊕ Create PROM File (PROM File Format             ⊕ Boundary Scan	→ → → → → → → → → → → → → → → → → → →	•
IMPACT Processes ↔ □	Add Device       Would you like to add another device file to Revision: 0 ?       Yes       0x00FF_FFFF	E .
	🛞 Boundary Scan 🛞 PROM File Formatter: SPI Flash Single FPGA	
Console	++□	8×
INFO: iMPACT: 501 - '1': Added I Add one device.	Device xc6vlx130t successfully.	~ ~ 4
PROM File Generation Target SPI	Flash 43,719,776 Bits used File: fecv6_adc_v100 in Location: D:\Documents\Local\FECv6_ADC\prom/	ns

h) Now, double click on the "Generate File ..." button

🛞 ISE iMPACT (P.20131013) - [PROM File Form	atter: SPI	Flash Sing	gle FPG	iA]	-	
Eile Edit View Operations Output	Debug	Window	/ <u>H</u> el	р		_ & ×
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MPACT Flows       ↔       ➡       ★         Image: SystemACE       Image: SystemACE       Image: SystemACE         Image: SystemACE       Image: SystemACE       Image: System		Rev0 PROM / FLASH	adc_!	0x0000_0000	128M	E
				0x00FF_FFFF		
		Bound	lary Sca	in 🎯	PROM File Formatter: SPI Flash Single FPGA	·
Console						⇔⊡₽×
Add one device.5367d1	)evice	xc6v1x	130t	successful		~ ~
PROM File Generation Target SP	Flash	43,719,776	Bits us	ed File: fecv6_	adc_v100 in Location: D:\Documents\Local\FECv6_ADC\	prom/ usb-hs

#### i) You will find the necessary mcs files in the desired location.



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Coover Cocuments	▶ Lo	cal ▶ FECv6_ADC ▶ prom	✓ <sup>4</sup> → Search prom		٩
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🔆 Favorites	<b>^</b>	Name	Date modified	Туре	Size
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🗼 Downloads		fecv6_adc_v100.mcs	12/08/2014 17:43	MCS File	14 6
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