FEC Firmware Upgrade Tutorial

1 FEC programming using the Xilinx Impact software

1.1 Installing the Xilinx Impact software

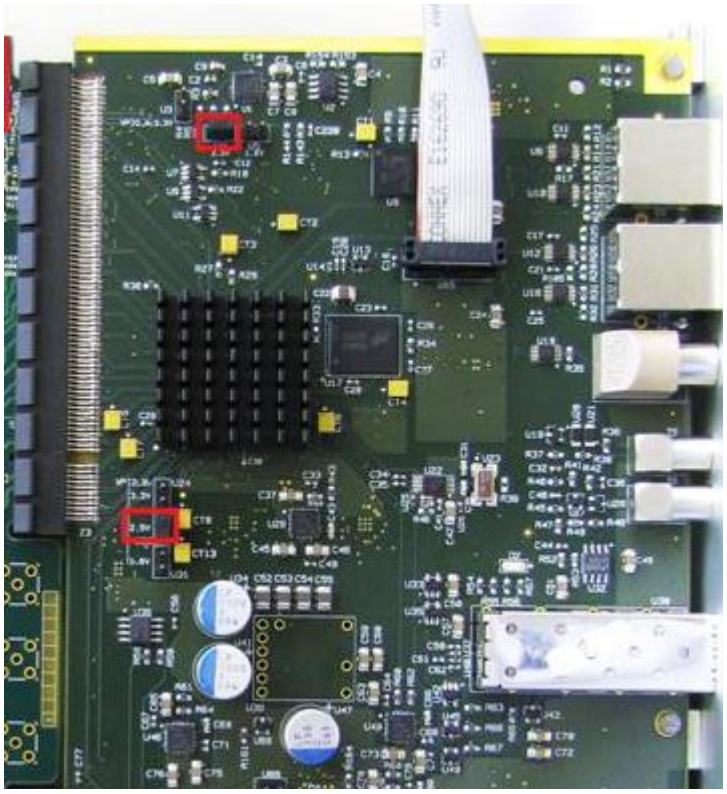
Go to the Xilinx.com website section Products -> Design Tools and download and install the free ISE WebPACK. If you have access to a full installation package (eg. CERN dfs) you can install the "Lab Tools" only, which will install Impact without the need to purchase or request a licence. The Xilinx software supports both Linux and Windows platforms.

You will also need to use the Xilinx Programmer cable (Platform Cable USB II)

You can find more information about alternative programming options from the Xilinx website, in the Products – Technology - Configuration Solutions section. In particular Digilent offers programming solutions compatible with the Xilinx software (for more details go to http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,395&Cat=5)

1.2 Connecting the Xilinx programming dongle to the FEC card

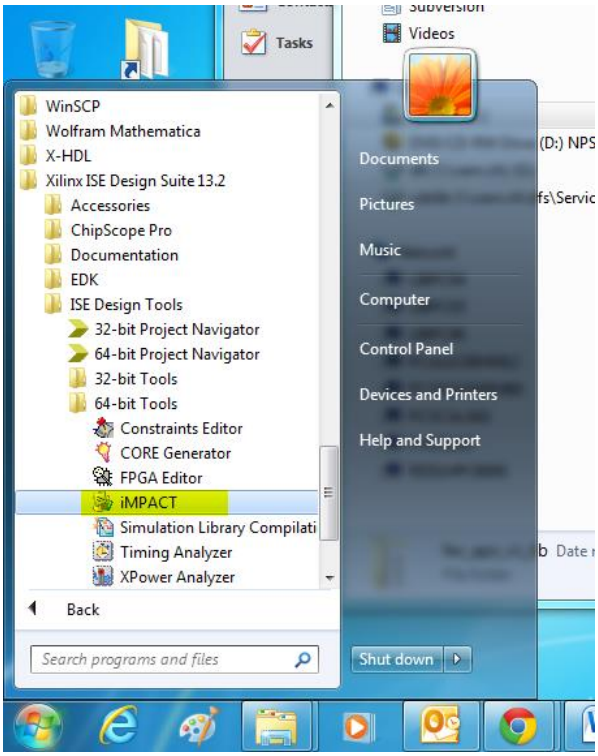
a) Connect the Xilinx Programmer to the PC and wait until it is recognized and the corresponding drivers are automatically installed (Windows)
b) Make sure the FEC card is switched off, then connect the flat cable of the Xilinx Programmer to the corresponding FEC connector (U15)



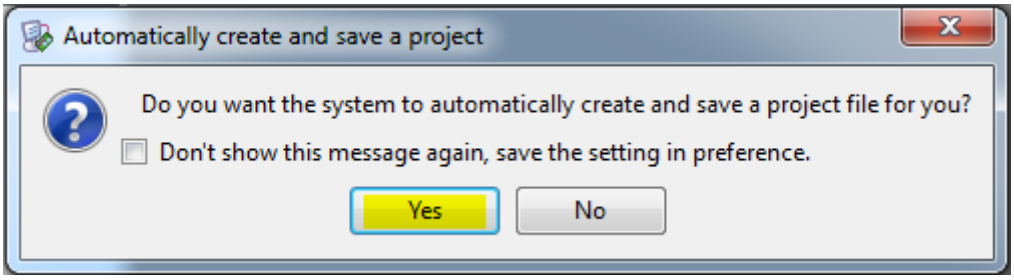
c) Power on the FEC card. If power conditions are ok, the light on the Xilinx Programmer will turn green.

1.3 Programming the FEC board

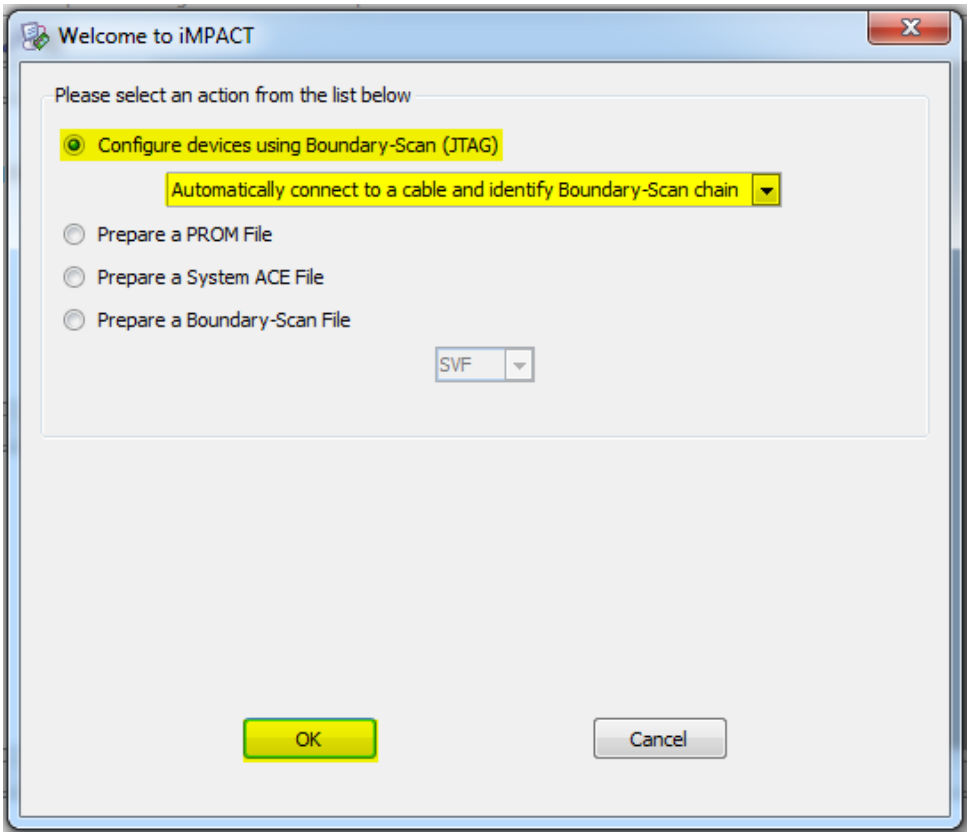
a) Start the Impact software from the Start Menu:



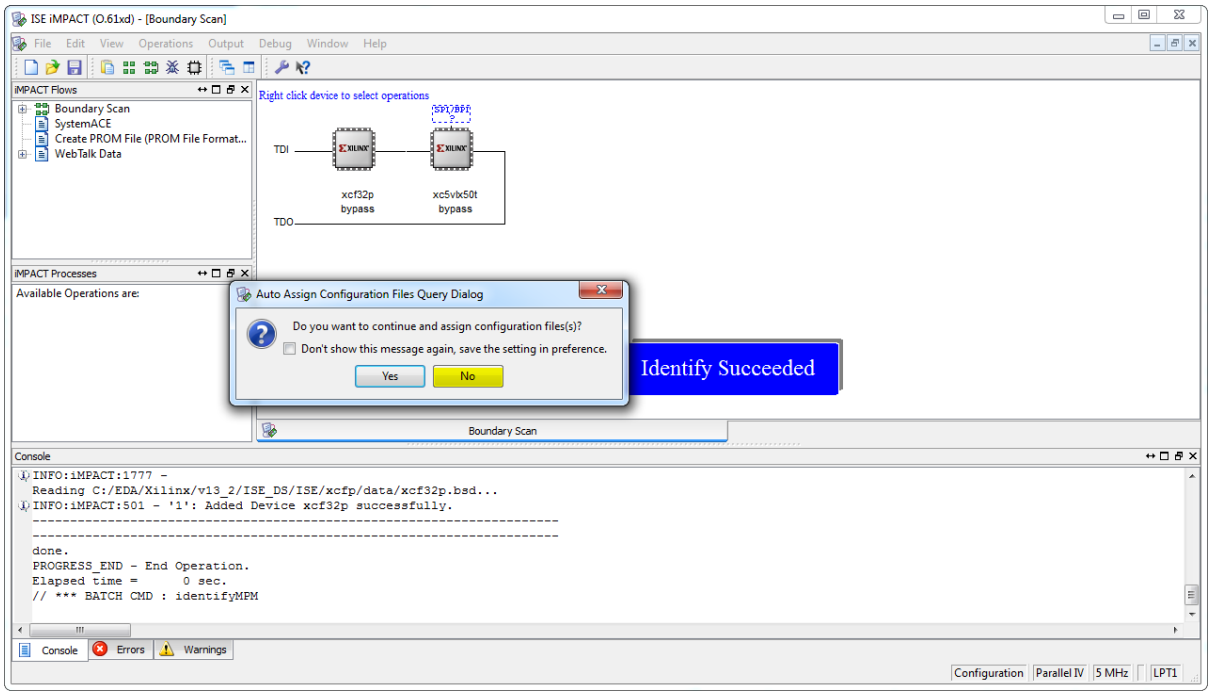
b) Answer *Yes* when asked to create a project



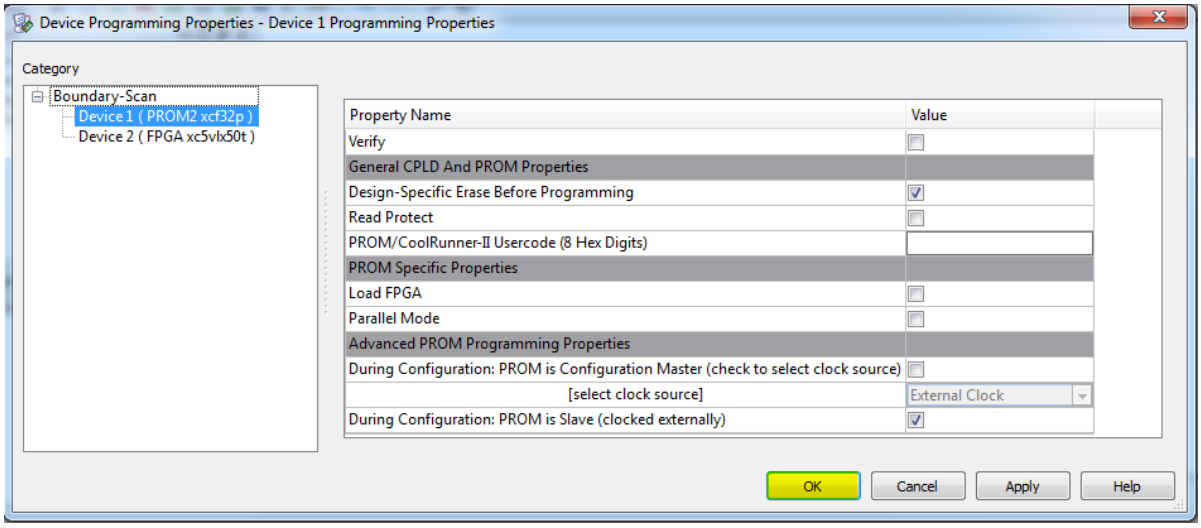
c) Make sure that *…Boundary-Scan (JTAG)* is selected and press OK



d) The program will automatically identify the devices EEPROM and FPGA devices present on the FEC JTAG chain. Press *No* when asked to automatically assign configuration files.



e) Press *OK* to accept the default programming parameters

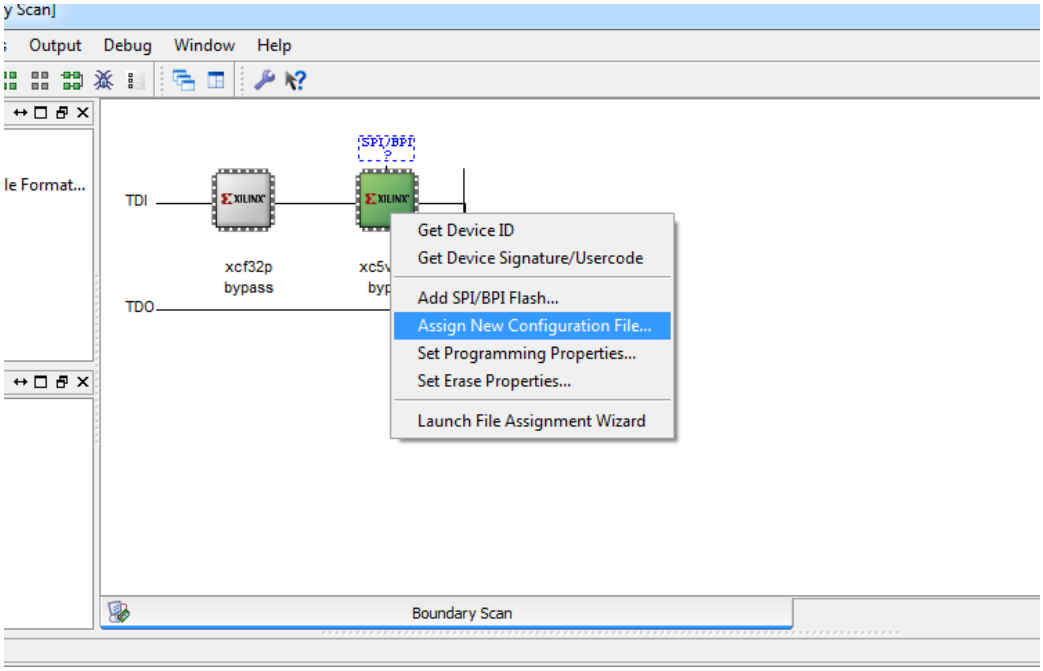


1.3.1 Temporarily programming the FEC FPGA

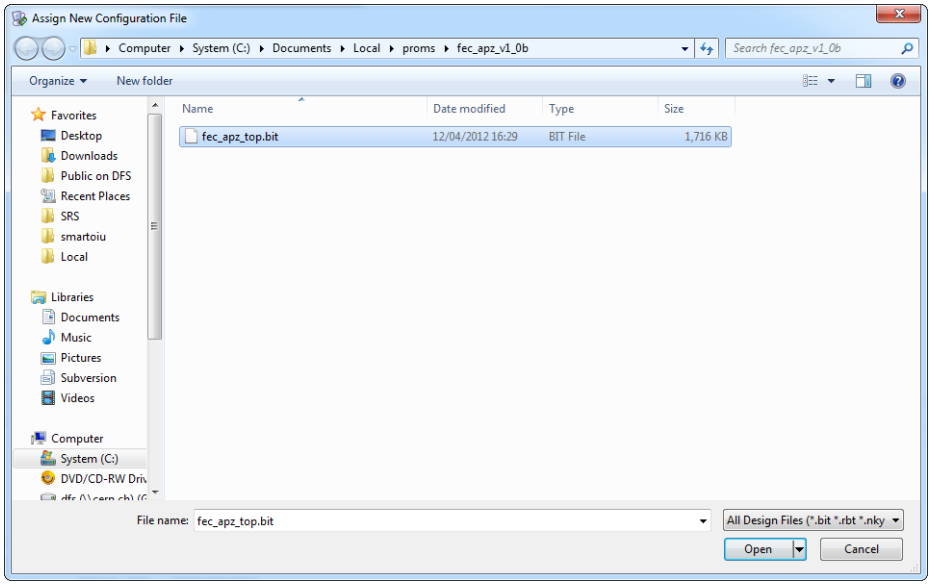
The firmware can be loaded directly into the FPGA without writing it permanently to the on-board EEPROM. This operation is useful for testing a new firmware update with minimum risk. At the next power cycle, the FPGA will boot with the default firmware stored on the local EEPROM. If you want to continue testing the new firmware you need to reload it to the FPGA.

If you want to permanently write the new firmware to the FEC board, go to next section (1.3.2 Program the on-borard boot EEPROM (permanent programming))

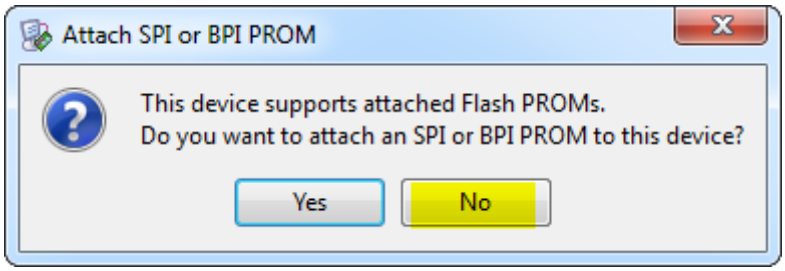
a) On the Boundary Scan tab right-click on the FPGA device (xc5vlx50t) and select *Assign New Configuration File …*



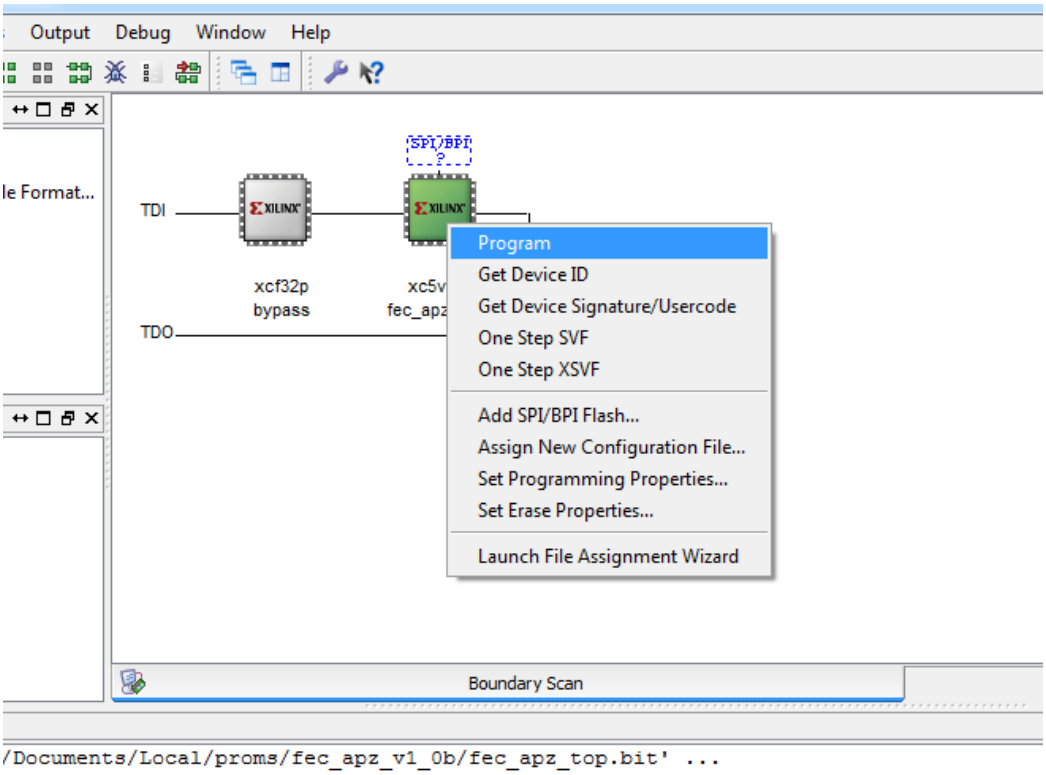
b) In the new dialog, select the *.bit* file corresponding to the new firmware from the location where you unpacked the zip file downloaded from the web.



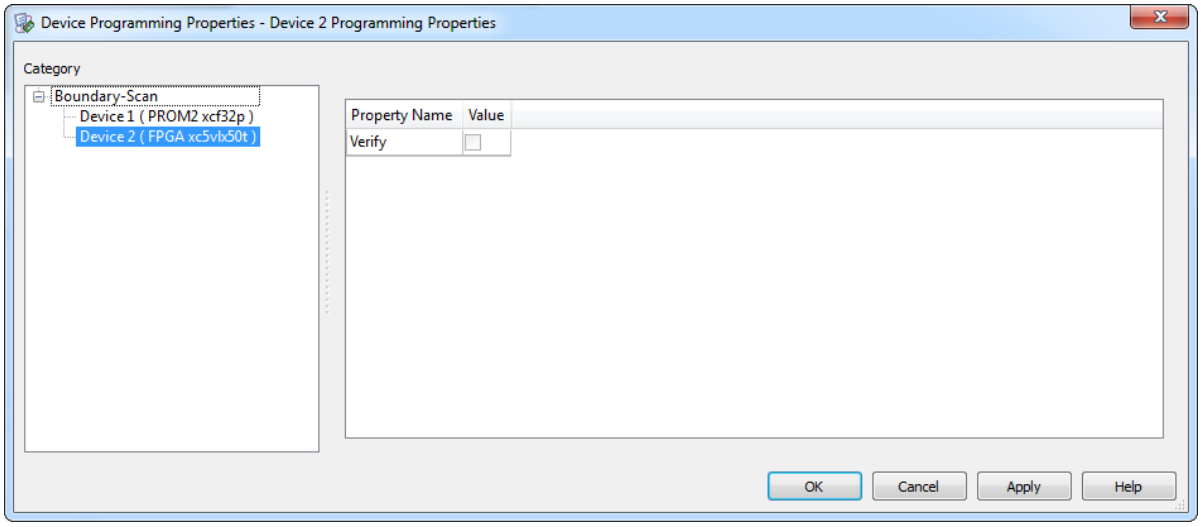
c) Press *No* when asked to attach a SPI or BPI PROM



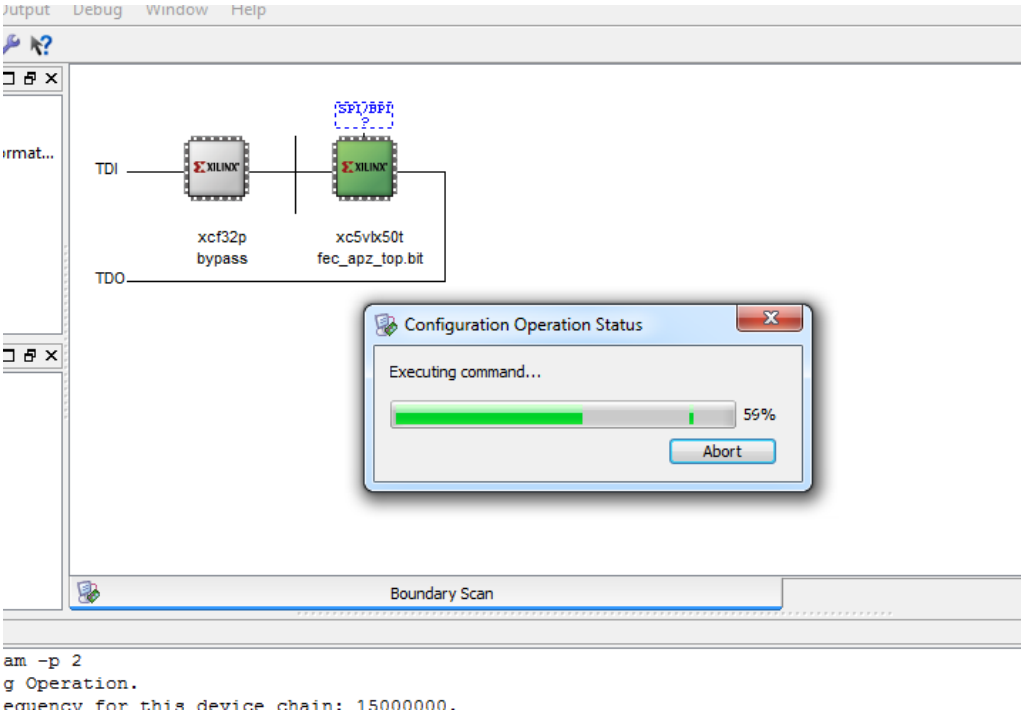
d) Right-click again on the FPGA device and select *Program*



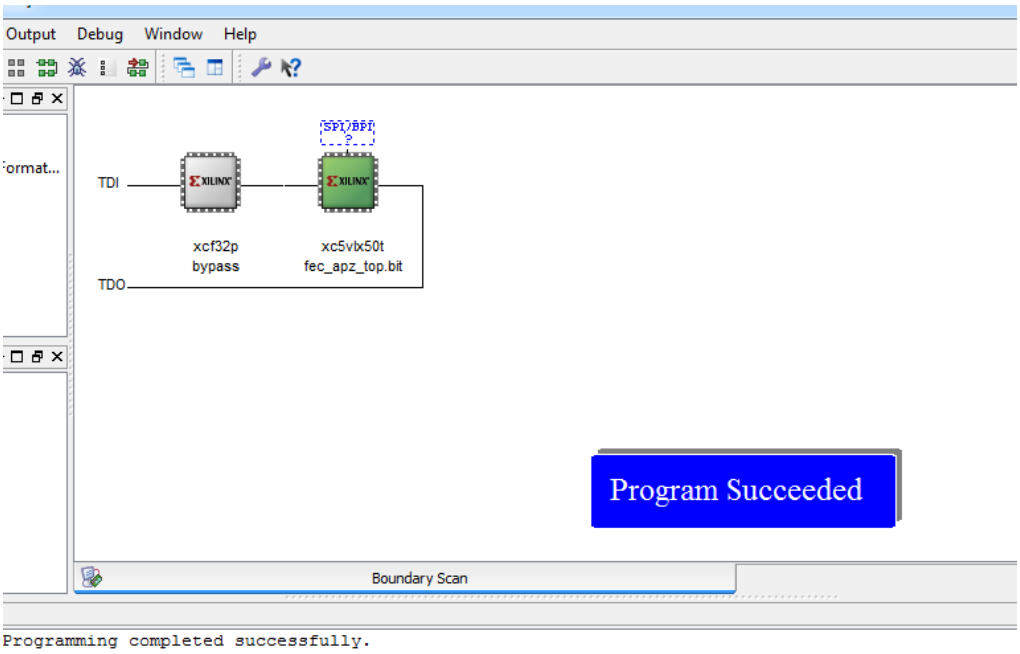
e) Click *OK* to accept the default programming properties



f) Wait until Impact loads the firmware to the FPGA

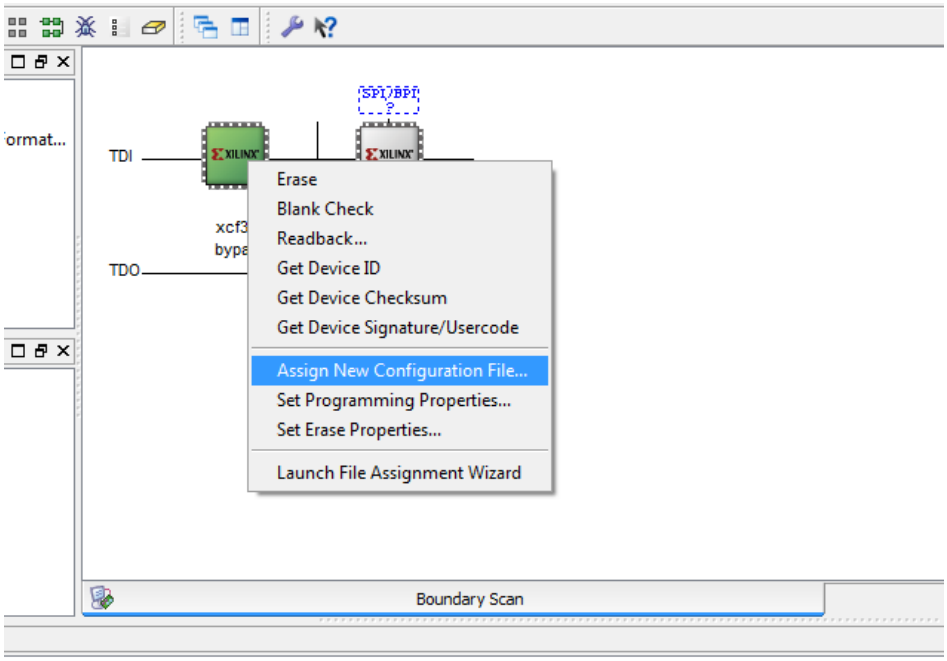


g) If the programing procedure was successful Impact will display “Program Succeeded”. You can now use the new firmware. Remember that the FPGA will revert to the old firmware after a power cycle or reboot command.

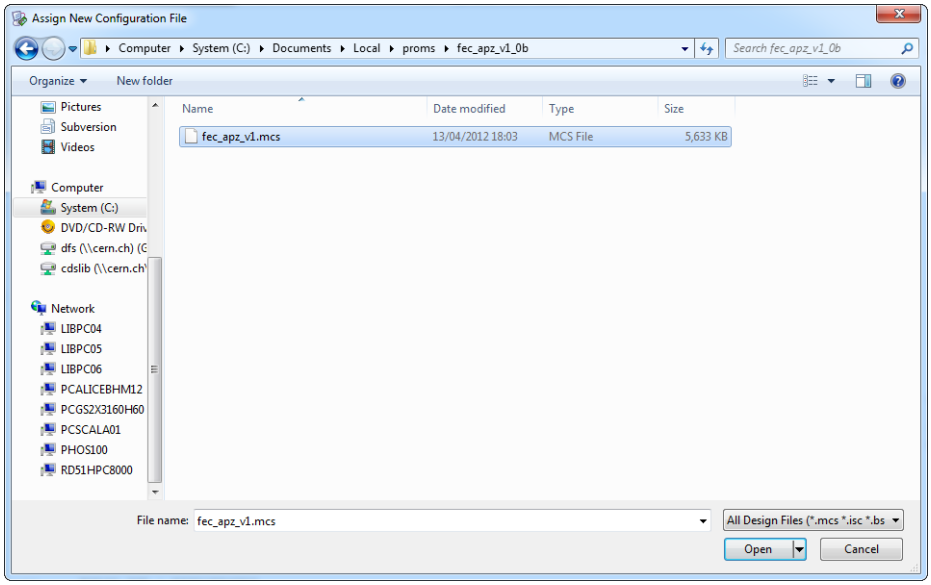


1.3.2 Program the on-borard boot EEPROM (permanent programming)

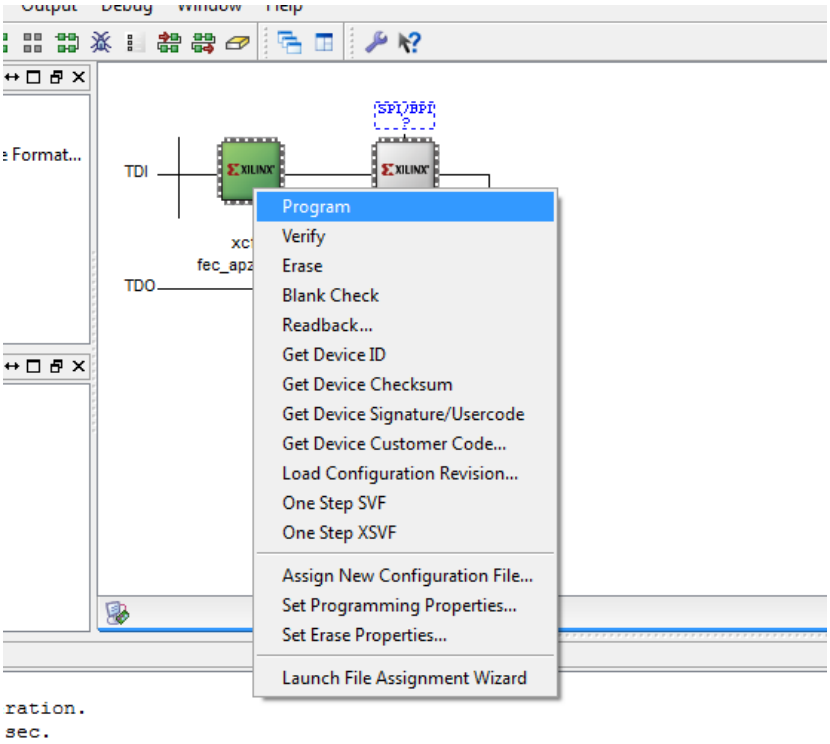
a) On the Boundary Scan tab right-click on the EEPROM device (xcf32pt) and select *Assign New Configuration File …*



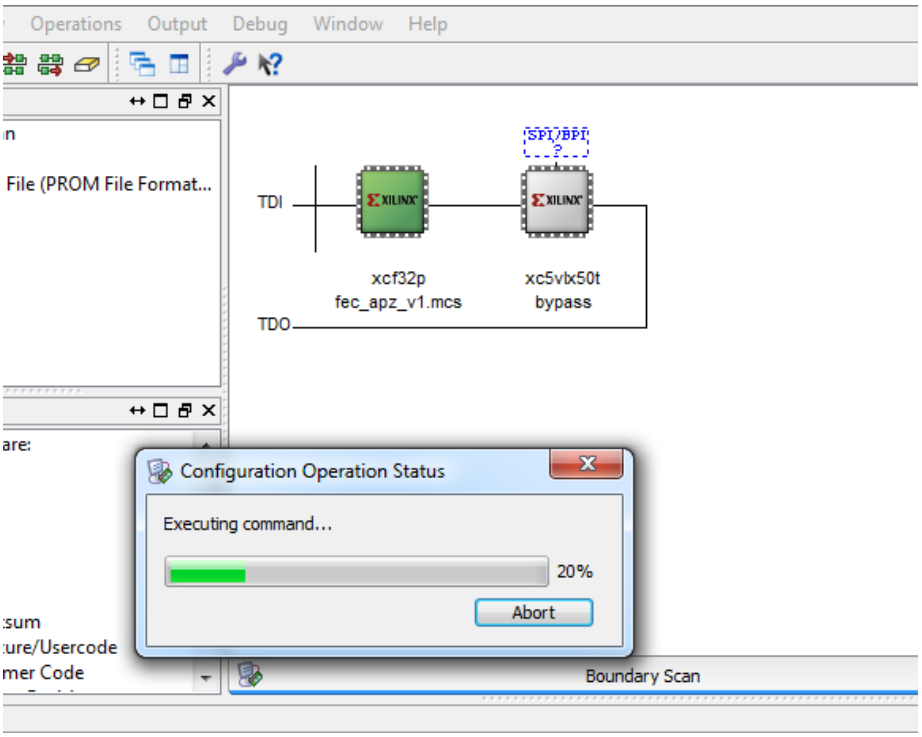
b) In the new dialog, browse to the location where you unpacked the zip file downloaded from the web and select the *.mcs* file corresponding to the new firmware.



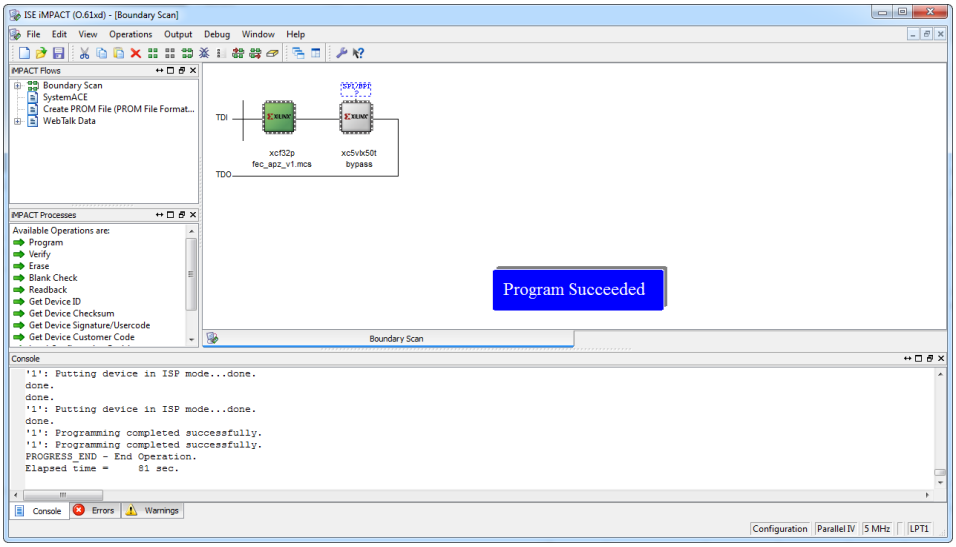
c) Right-click again on the EEPROM device and select *Program*



d) Wait until Impact loads the firmware to the EEPROM



e) If the programing procedure was successful Impact will display “Program Succeeded”. You can now power cycle the FEC board to load the new firmware from the boot EEPROM.

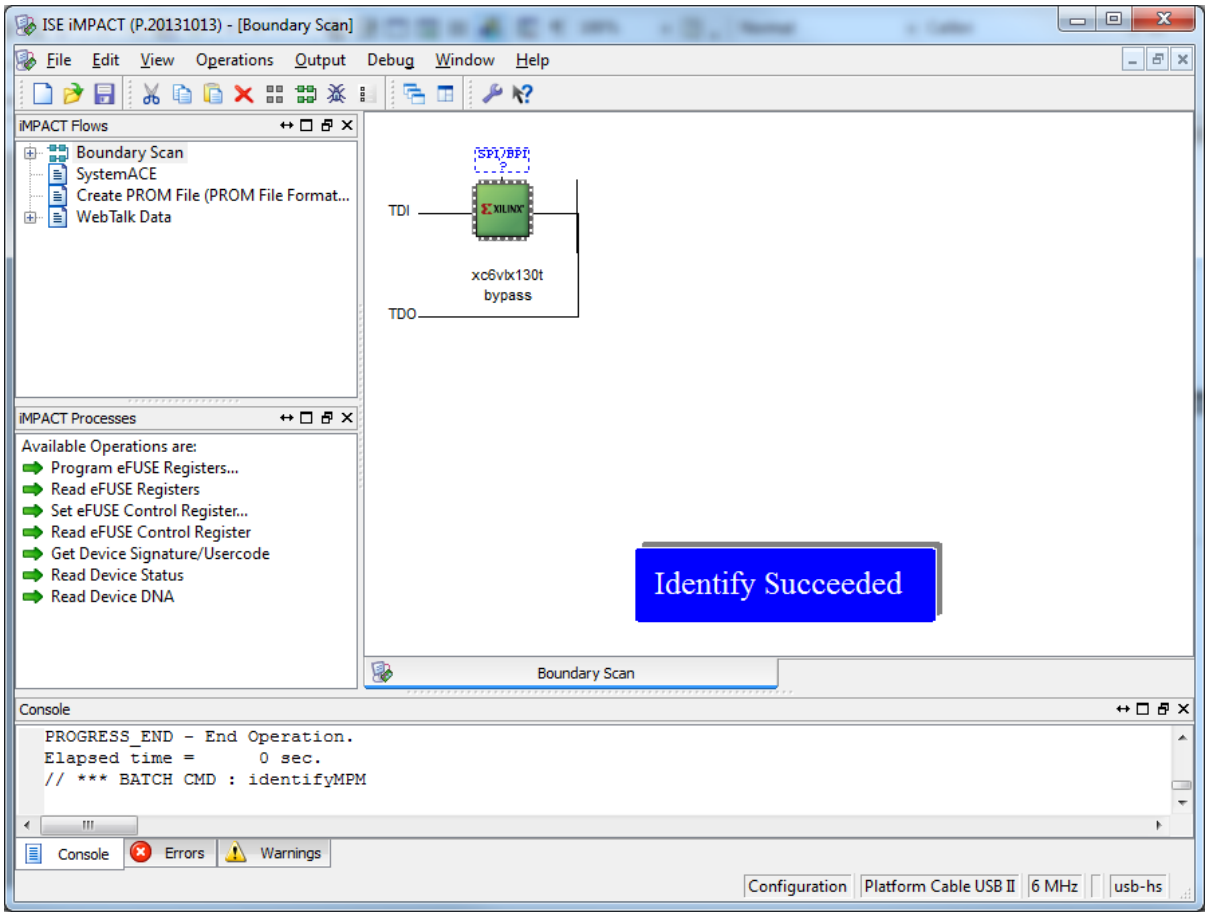


1.4 Programming the FECv6 board

The JTAG connection of the FECv6 board is on the front-panel of the board, below the two DTCC RJ45 connectors.

... picture ...

To start the Impact programming tool you have to follow the same procedure as for the FECv3, as described in chapter 1.2. In this case, the main window of the tool will look like this:



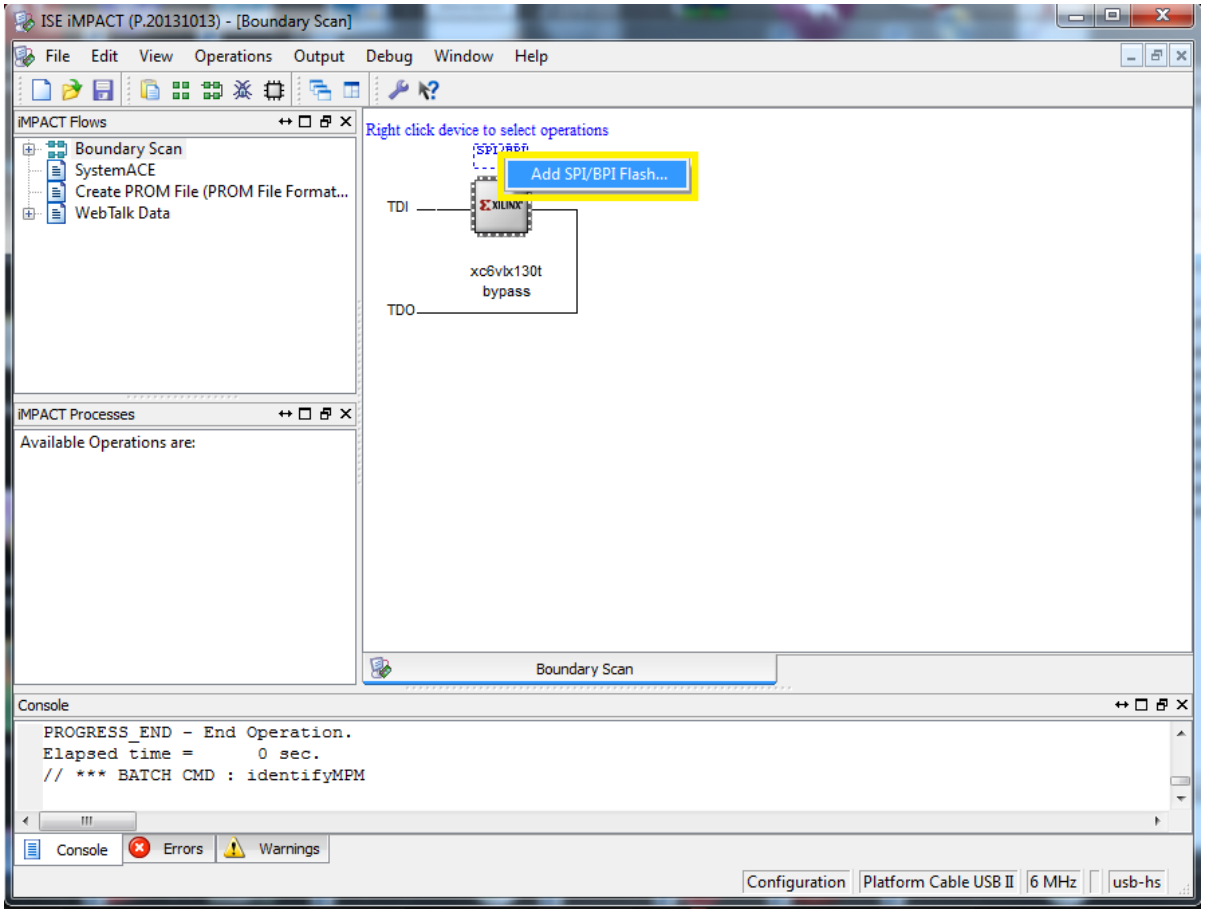
1.4.1 Temporarily programming the FECv6 FPGA

The procedure is identical with the one described in chapter 1.3.1

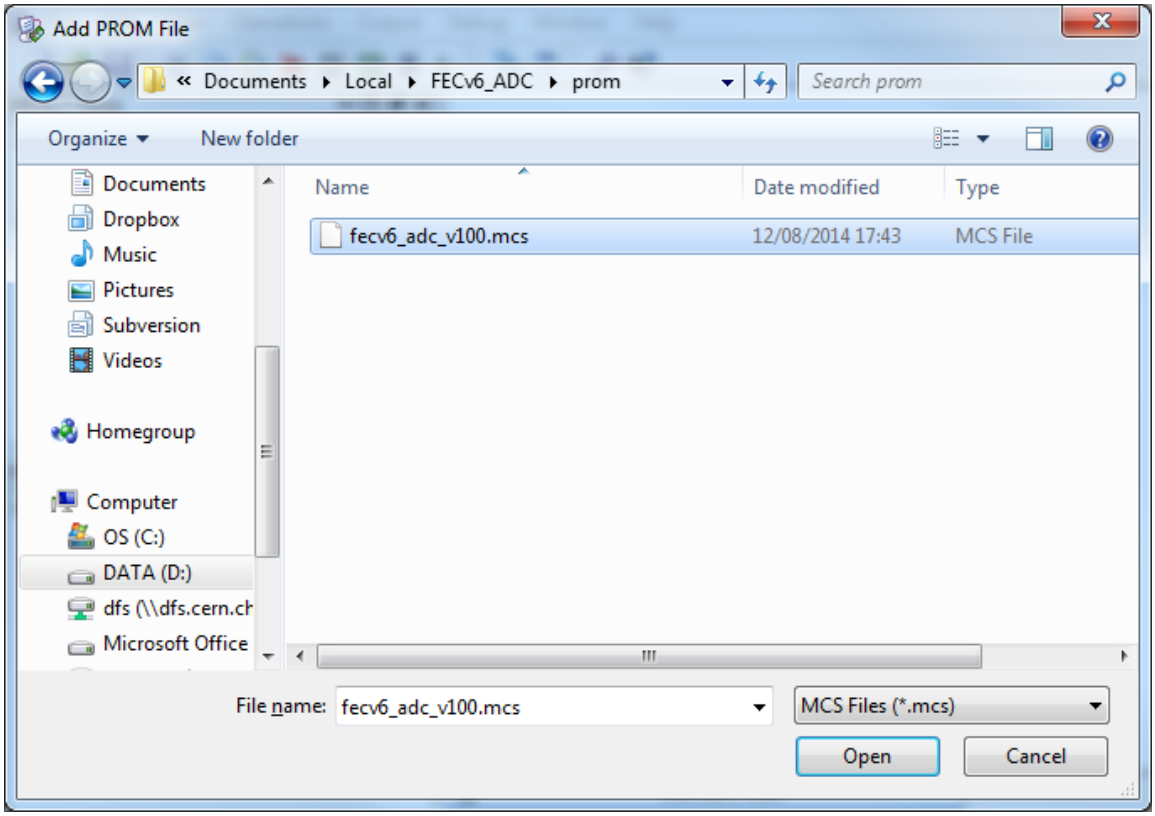
1.4.2 Program the on-borard boot EEPROM (permanent programming)

The FECv6 board uses a SPI flash chip which is not automatically detected by the tool.

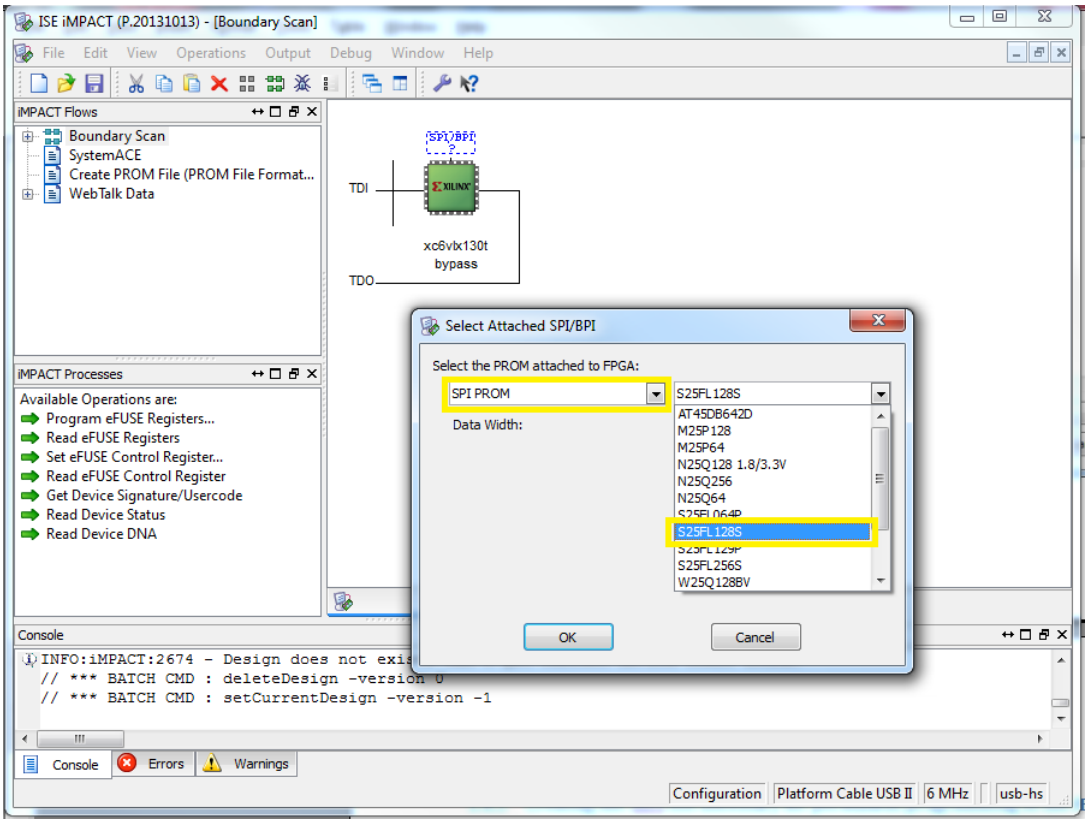
a) Right click in the dotted rectangle on top of the FPGA icon where it is written "SPI/BPI ?", then click on the "Add SPI/BPI Flash..." menu item.



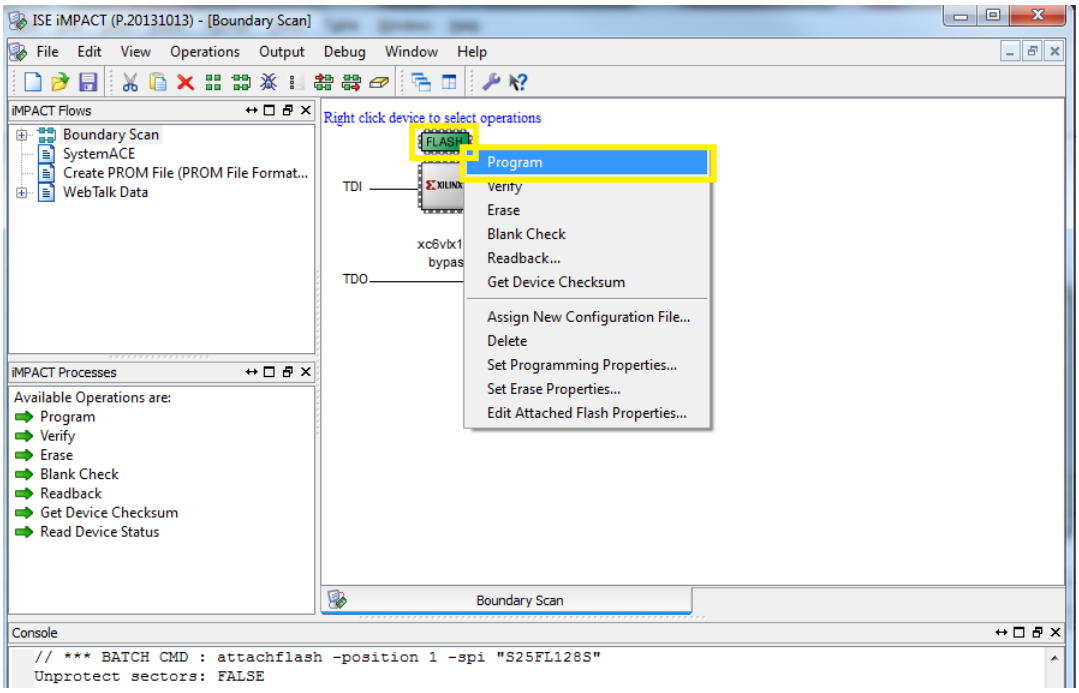
b) Select the .mcs file for the SPI programming



c) Leave "SPI PROM" as the type of PROM attached to the FPGA, and select the PROM part number from the drop-down list (the default prom used with the FECv6 board is S25FL128S; select another one if your board does not use the default one.)



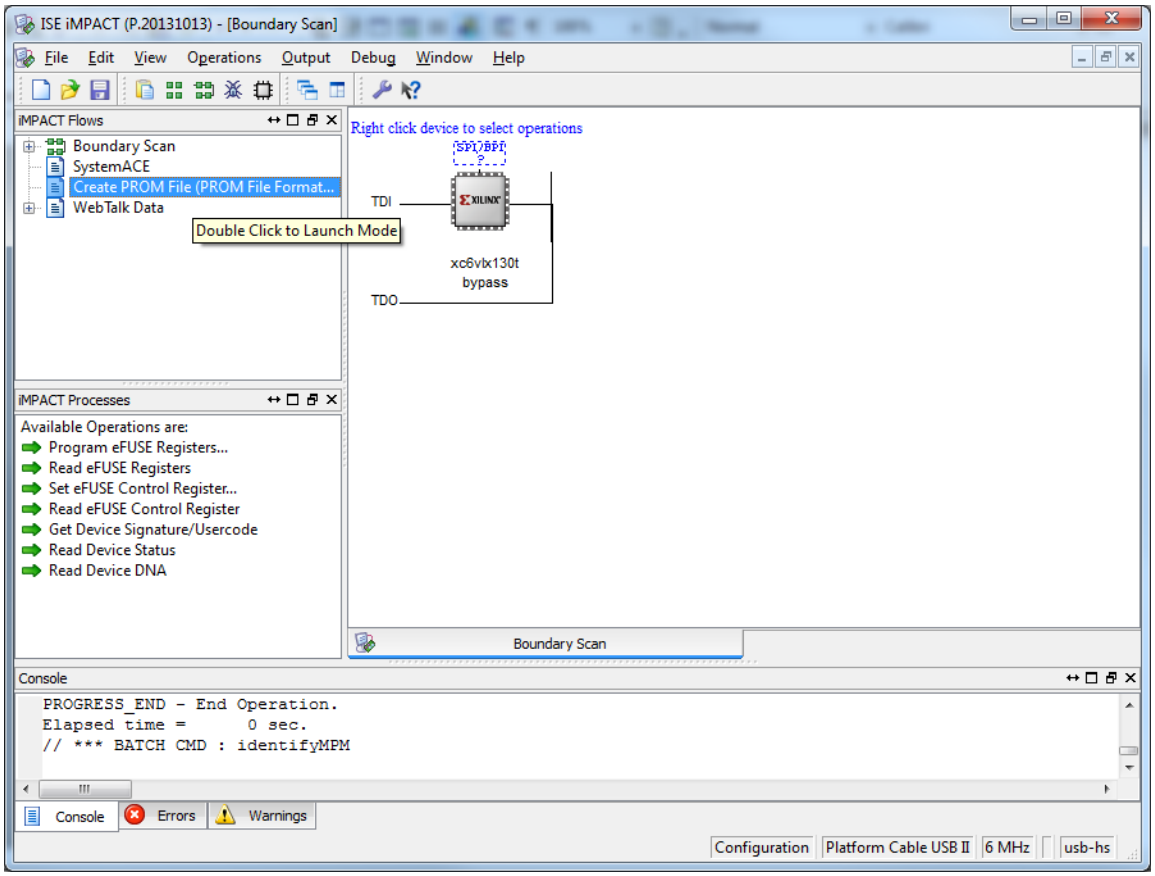
d) Right click on the "FLASH" icon and select the "Program" menu item, then click "OK" in the Device Properties window. This will start the programming of the SPI flash. Do not power off or unplug the programming cable during this process.



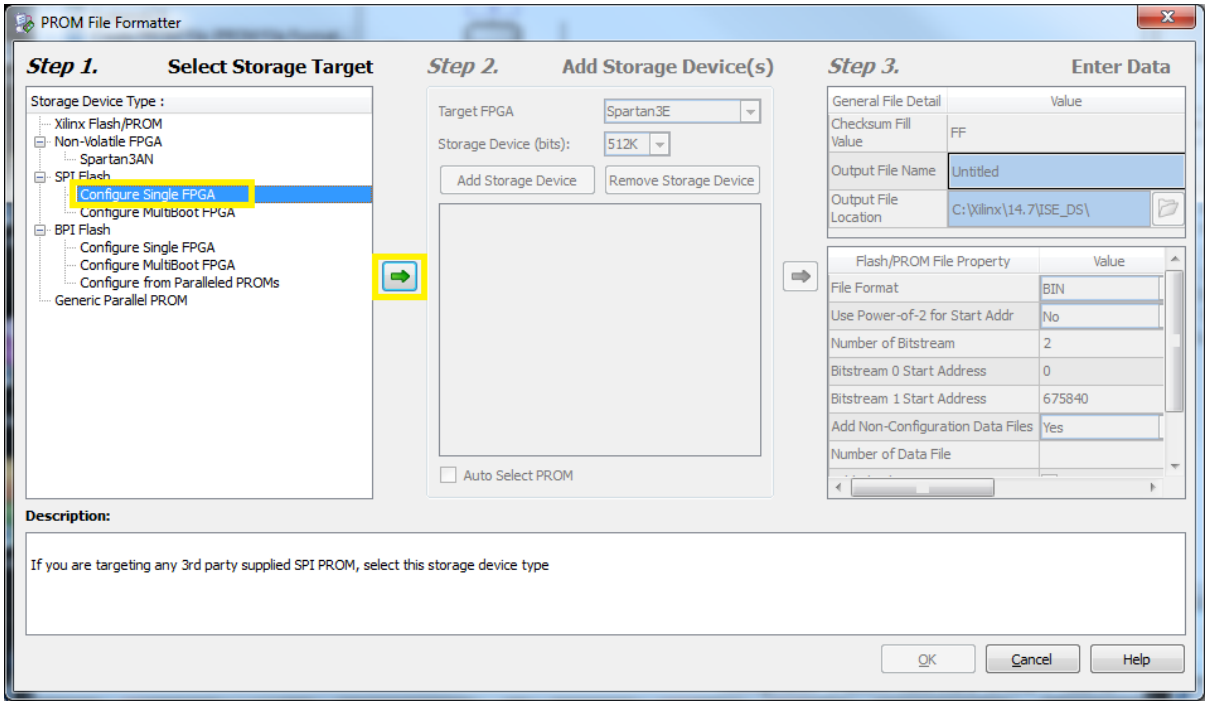
1.4.3 Creating the .mcs file necessary for permanent programming of the FECv6 board

If you do not have the .mcs files necessary to program the on-board SPI flash, or you have a different SPI flash, use the following procedure

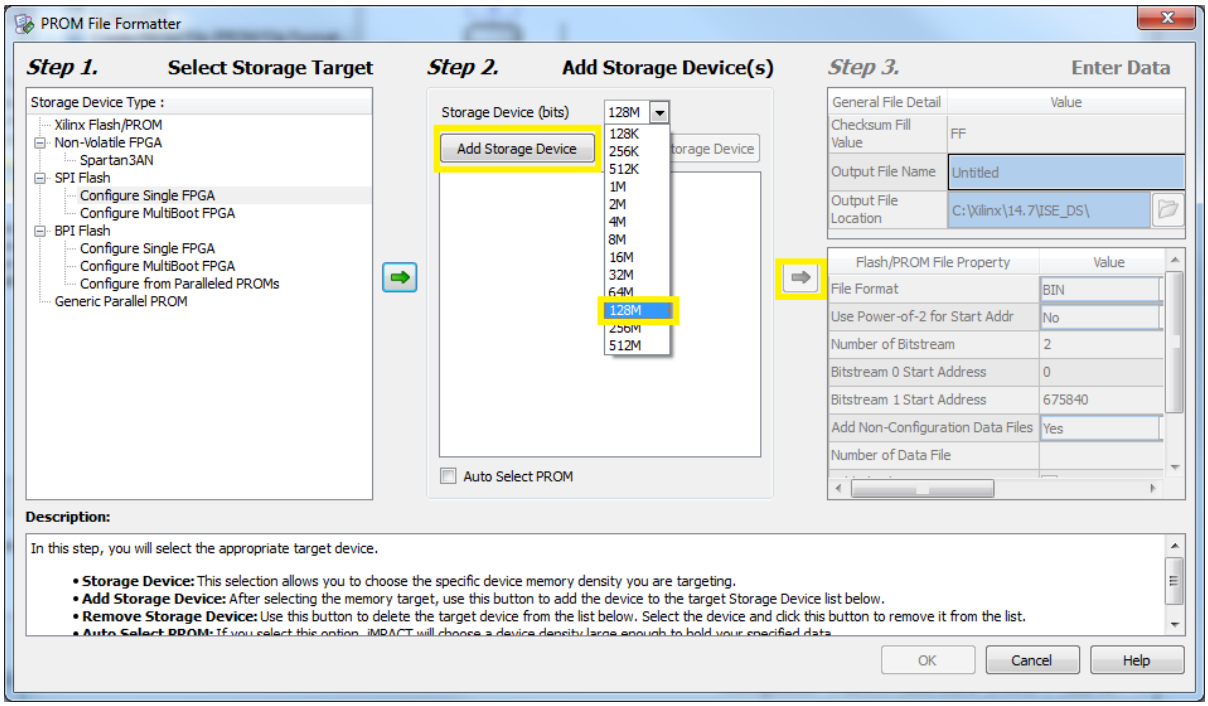
a) Open the ISE Impact tool and double click on the "Create PROM File (PROM File Format..)" item in the Impact Flows list of the ISE Impact tool.



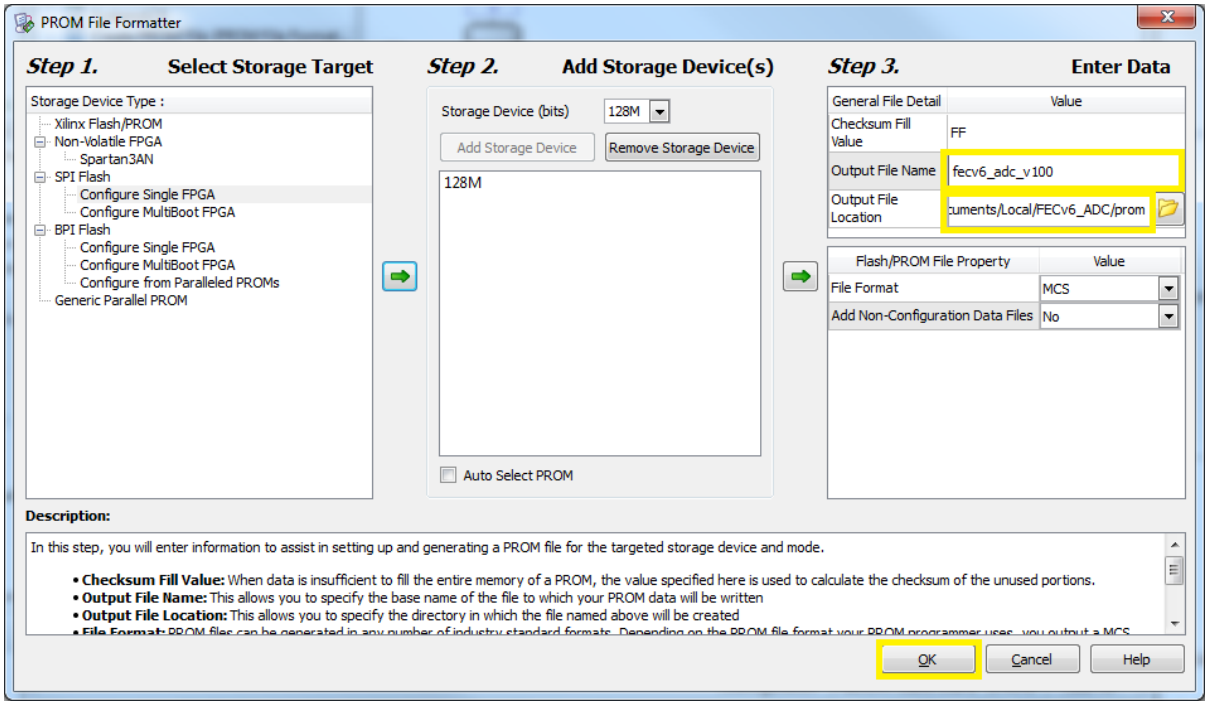
b) Select the "Configure Single FPGA" item under the "SPI Flash" category of Step 1, and then press on the green arrow on the right.



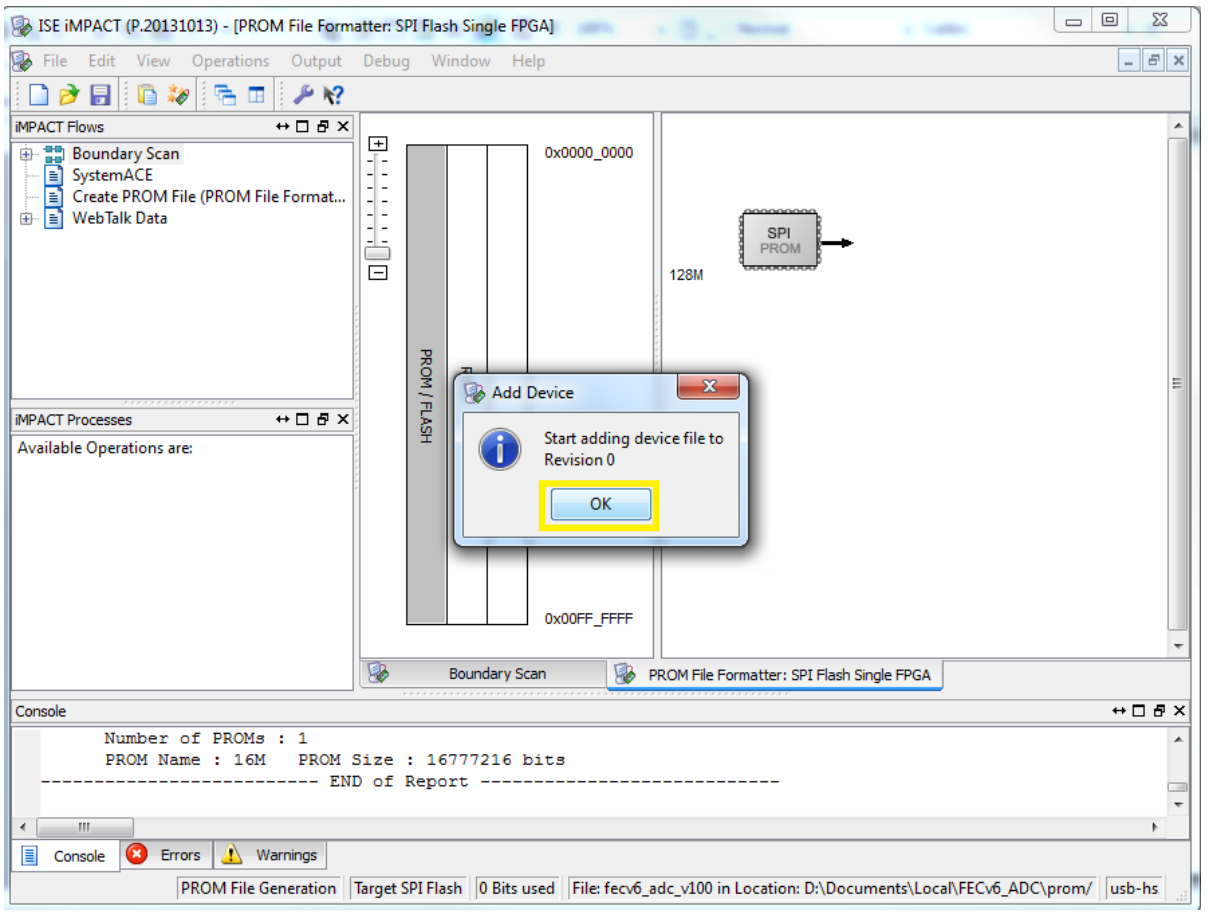
c) Select "128M" in the "Storage Device (bits)" list and then click on the "Add Storage Device" button followed by the green arrow button on the right.



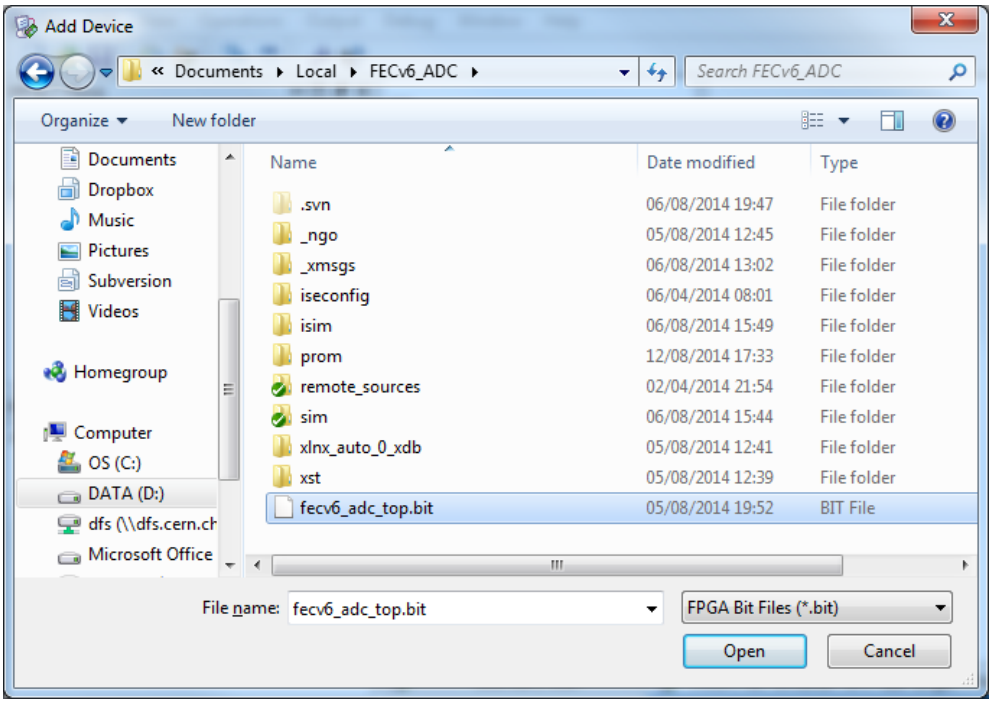
d) Change the "Output File Name" and "Output File Location" to the desired directory, then click OK.



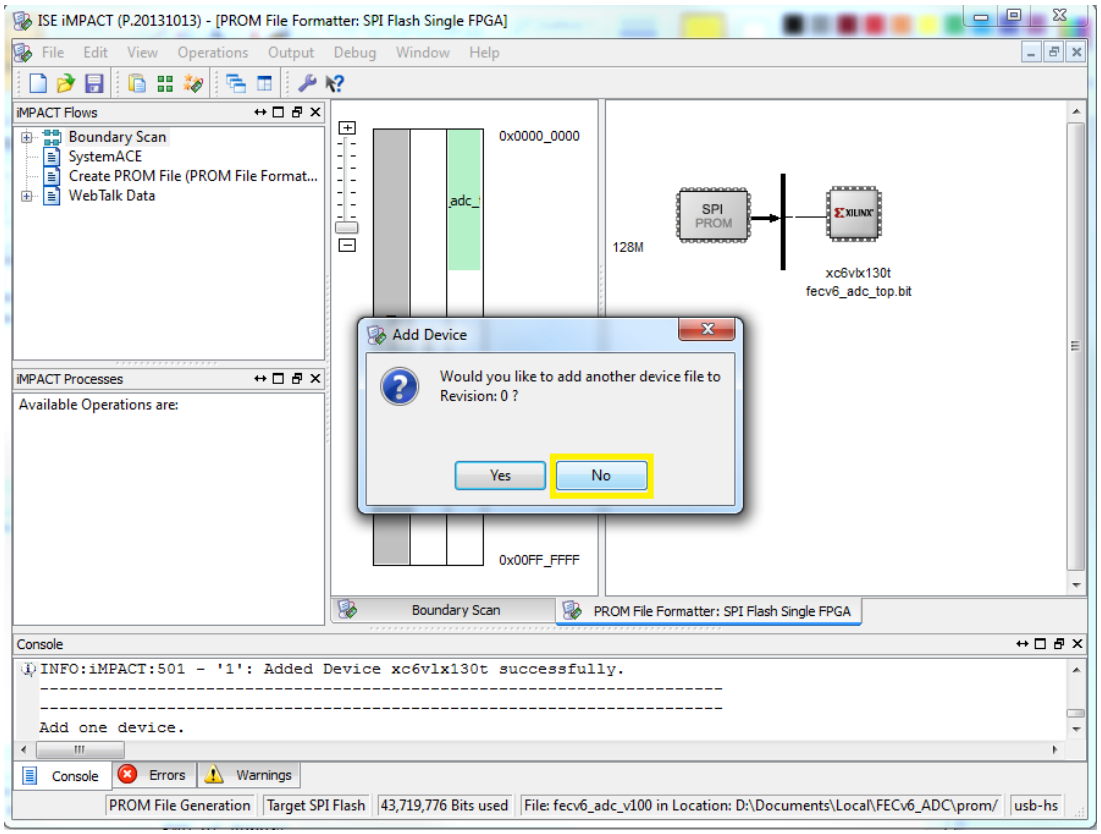
e) Click OK to start adding the device file:



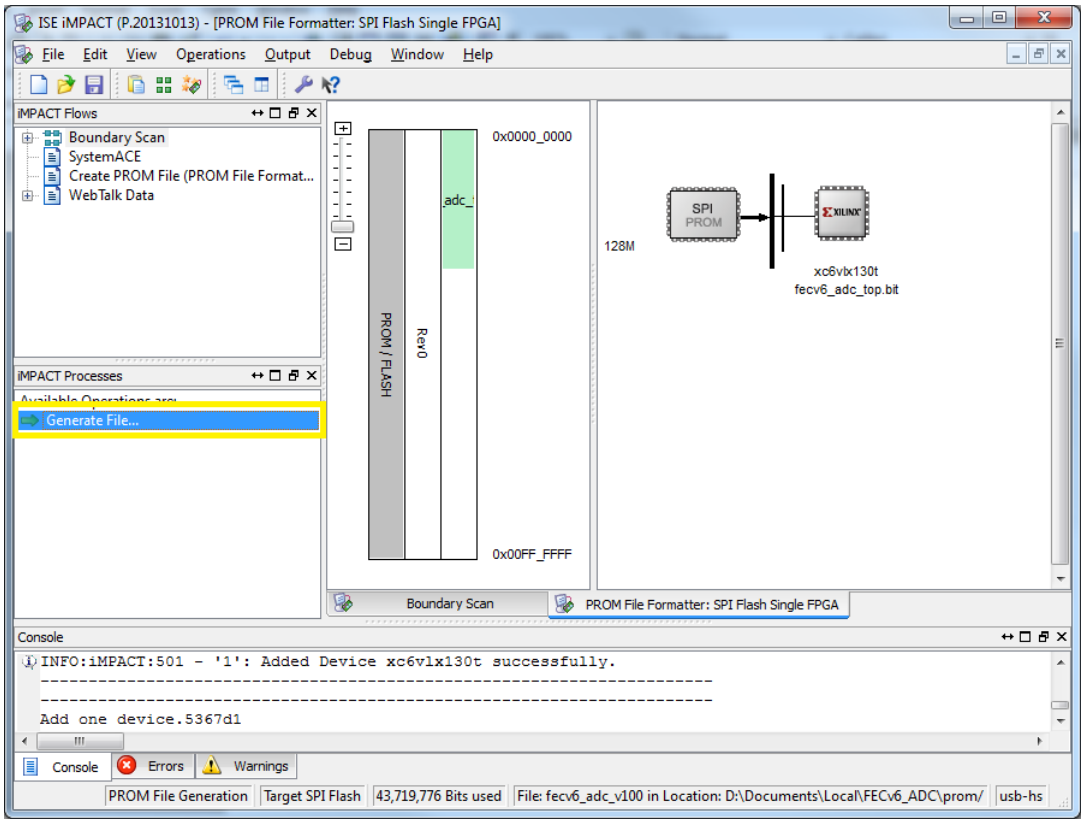
f) Select and open the desired bit file



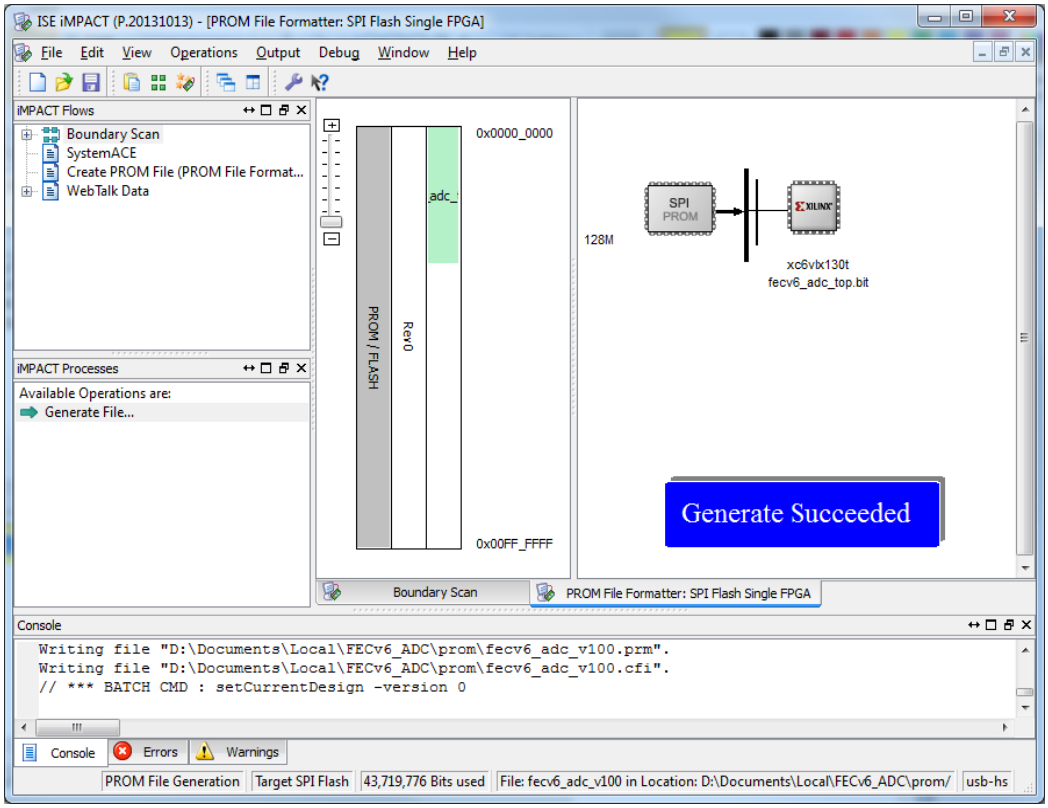
g) Click "No" to finalize the process of adding the design file

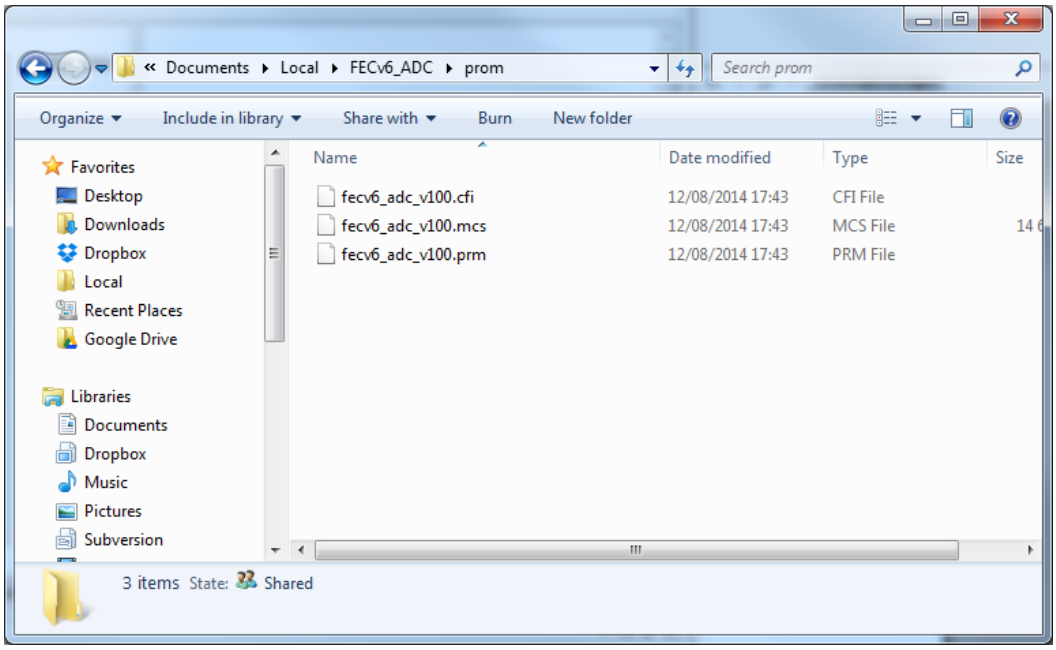


h) Now, double click on the "Generate File ..." button



i) You will find the necessary mcs files in the desired location.

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Dropbox
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Pictures
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PRM File
3 items State: Shared